RAPID PROTOTYPING USING LASER RESTRUCTURABLE VLSI CIRCUITS

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ABSTRACT

The development of *Application Specific Integrated Circuits* (ASICs) is a costly proposition in terms of the technology, equipment, and the time required. For small companies, developing ASICs is cost prohibitive. The advent of *Laser Restructurable VLSI* (LRVLSI), promises the design engineer the capability to interconnect cells that implement generic logic functions (e.g., sum of products) to achieve a higher level of complexity design. At the *Center for Microelectronics Research* (CMR), an operating environment and infrastructure for rapid prototyping and quick turnaround using laser restructuring of VLSI circuits were developed. The purpose of this facility is threefold: to pursue research on novel interconnect technologies using LRVLSI, to develop the capability of operating in a quick turnaround mode using optimized process parameters, and to maintain standardization and compatibility with commercially available equipment for feasible technology transfer. The system was developed to research fundamental interconnect technologies and to develop production controls for the use of the technologies. The goals of the system were to possess a high degree of flexibility, high data quality, total controllability, full documentation, short downtime, an operator-friendly interface, automation, historical record keeping, and error indication and logging. Standardization and compatibility with existing equipment are achieved by using only off-the-shelf hardware and software platforms. This was done throughout the design of the system.

I. INTRODUCTION

It can typically take twenty days or longer to obtain the first batch of prototype chips for an ASIC product. For small companies, developing ASICs is cost prohibitive. With LRVLSI, it is possible to reduce this time frame to a matter of hours; and it can be done in house by minimally trained personnel or the designer if necessary. This quick turnaround feature promises to boost productivity and lower costs by reducing the time to market. The goal of LRVLSI would allow design engineers the capability to interconnect cells that implement generic logic functions (e.g., sum of products) to achieve a higher level of complexity design. Figure 1 shows a conceptual approach to LRVLSI; where N generic logic networks can be connected to form a one dimensional input-output path using N+1 interconnect networks. The logic blocks can be different, and can contain combinatorial and/or sequential logic. The interconnect networks can be the same general purpose interconnecting cell. This approach can be extended to two dimensions; it is limited only by area; and it efficiently adapts to digital signal processing applications where regularity, modularity, and parallelism are common characteristics of the system design.

II. INFRASTRUCTURE

A. Lab Set-Up

The basic laser system (Figure 2) consists of a high energy 5 watt Argon CW laser, an *electro-optic shutter* (EOS), an optic delivery system, and a high precision x-y-z translation stage. All the system components are mounted on a 2-ton granite table installed on four self leveling pneumatic legs for a vibration free process environment. The laser beam is pulsed by the EOS and is guided through the optic

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Table 1 - System Capabilities

PARAMETER	SPECIFICATIONS
X-Y Maximum Travel	4.00 inches
X-Y Full Travel Position Accuracy	0.254 μm, maximum
X-Y Repeatability	0.18 μm, maximum
X-Y RMS Noise Level At Position	±2 counts
X-Y Travel Speed	0.75 inch/s
Focus Control (z axis resolution)	0.1 μm
Laser Power (multi-mode)	0.30 W ~ 5.00 W
Pulse Width	2 μs, minimum
Pulse Period	3 μs, minimum
Number of Pulses	1 ~ 9999

delivery system where the beam is focused down, by means of a 50x objective lens, to a minimum spot size between 2 μm and 3 μm. The laser beam is then directed to a chip mounting set-up or a wafer chuck, depending on whether a chip or a wafer is being restructured. This apparatus is, in turn, mounted on a high precision x-y-z positioning system (position absolute accuracy is less than 0.5 μm of the commanded position over the entire range of travel). The x-y section consists of a linear induction motor x-y table with laser interferometer position feedback; and the z axis consists of a stepper motor and optical encoder combination with resolution of 0.1 μm, which gives the capability of fine laser focus. The chip mounting set-up or the wafer chuck sits on a tilt stage that is used to electronically level the surface and give it an approximate rotational orientation. A video camera system is used to observe the surface being restructured; and a relay actuated blocking shutter is also in place for safety. There is also a *digital multimeter* (DMM) in the system that can be readily connected to the chip containing the structures being investigated. If the terminals of these structures are accessible through the package pins; the experimenter can measure resistances in real-time for instant feedback, or the resistance values can be saved to a file along with the instantaneous operating parameters for analysis at a later time. One use of this feature would be for short screening runs where the amount of collected data is not significant and immediate evaluation of setup or parameters is needed. Otherwise, parts are parametrically tested by an HP4062B test system with Electroglass wafer prober or by a high speed digital HP82000 system. In addition, a 65 watt excimer laser is available. The optical heads for each laser are mounted on a common rail, and can be switched and fixed into place. The impact of a Nd:YAG laser is also being explored for incorporation into the lab. This will give the laboratory a high degree of flexibility and a wide spectrum of capability from the deep uv to the far infrared.

The laser system is controlled by a DOS based 486DX PC, with every parameter in the system controlled and observed by the researcher. Parameters are: x and y positions, focus (z position), laser power, laser frequency, duration of laser pulse, period of the pulses, and number of pulses.

B. Control Software Environment

The Lab Windows environment by National Instruments was chosen for the development system. All control software was written in a subset of the C programming language, utilizing the power of readily available plug in boards which provide resources such as: counters, timers, AD/DA

converters, IEEE-488 interfacing, and digital I/O. Most of the instruments use IEEE-488 for communications, but in some cases digital and/or analog control is required (e.g., generating a series of pulses to control the EOS). Some features of the control program are process error warning and logging, and maintenance scheduling. The latter is achieved through the program's constant monitoring of the actual process parameters. If a parameter is not within the specified tolerance range of the commanded parameter, the researcher is notified; thus, helping in scheduling of maintenance and repairs.

With the considerable task of controlling everything from sub-micron motion to high power laser zaps and monitoring the many possible parameter and status sources, Lab Windows proved to be invaluable. The control environment exhibits a high degree of consistency with widely accepted visually programmed graphical "point-and-click" interfaces. Fill-in-the-blank prototyped functions provided the researcher, with a modest knowledge of C, the ability to explore the full range of the system's capabilities. The program and interface screen can easily be reprogrammed and/or reconfigured to accommodate new needs due to technology advancement or component upgrade. There is ample room for evolution of the control software to encompass process statistical control using built-in functions. Examples of this would be to dynamically graph parameters and make adjustments based on user input or the accumulated knowledge base for the particular process.

C. Optimization of Process Parameters

To optimize the parameters of the laser linking and cutting process, a statistical process control approach was chosen (Figure 3). The software tools used were the statistical packages RS1 and SYSTAT. One link structure was studied, *Laser-Diffused Links* (LDLs)[1] with and without passivation; and metal 2 cuts were also studied. Preliminary experiments were designed by RS1 using 5 levels of each parameter. Normally 5 levels are not used in experimental design; however, the extremes for the parameters were not understood in this case. The parameters varied were focus, laser power, pulse duration, and number of pulses. The laser used was the argon laser with multi-mode wavelengths; although single wavelengths are also available, and its effect will be investigated in the future. The period was set to be twice the pulse duration, resulting in a constant 50% duty cycle.

After the preliminary experiments were carried out the chips were tested. The individual links and cuts were tested by forcing a voltage across them and measuring the current, also leakage to substrate was measured. The current data points were then fed into the statistical software where I-V curves were constructed; tested for linearity to detect diode-like behavior; and used in the construction of a statistical model and a response surface analysis, predicting the values of the process parameters to obtain the desired results. The failure modes that were investigated were high resistance or diode-like behavior for the LDLs, leakage currents of more than 1 nA for the cuts, and shorts to the substrate for all. Minimization of the restructuring time was also a criterion. Observed failure modes were high resistance for the LDLs, shorts to the substrate, and non opens for metal cuts. The results of the response surface analysis can be used to tune the next experiment which is designed to analyze yield and repeatability, a Taguchi analysis.

It is important to note that throughout this experimental cycle, vast amounts of data were collected, and that it was all done in electronic media. No human interaction was needed for data handling, other than running the tester, executing the statistical programs, and analyzing the results. The data from the tester was collected in the hard disk drive of the tester's computer, and then electronically transferred to a Unix network and DOS floppy disks for data analysis with the statistical programs.

We give bellow, in Table 2, the resulting optimum process parameters for the structures investigated. A positive focus is interpreted as moving the chip or wafer up, toward

Table 2 - Optimum Process Parameters for Structures Investigated

PARAMETER	LDL WITH PASSIVATION	LDL WITHOUT PASSIVATION	METAL 2 CUT
Focus	1.5 μm	1.6 μm	3.0 μm
Laser Power	1.38 W	1.44 W	2.00 W
Pulse Duration	35 μs	35 μs	30 μs
Pulse Period	-	70 μs	60 μs
Number of Pulses	1	6	150

the objective, from the zero reference which is being focused to metal 2. The positive focus values for the LDLs intuitively make sense; since once the chip or wafer moves up, the optics will be focused to diffusion. Figure 4 shows the distributions of the link resistance obtained with these parameters.

D. Running Parts

After the process parameters for a particular link or cut structure have been optimized in the research mode, the technology can be applied to an actual device. Script files can be generated from the layout design and then input to the laser system controlling software, thus specifying coordinates where the links and cuts should be made. Another way of creating the script files is using point and click while looking at the chip mounted in the laser table. The position can be selected, as well as the laser operation (link or cut). This gives a visual programming capability for creating script files. The script files generated using this method can then be used for many chips (same part), since it is independent of the particular chip mounted on the laser table and of the alignment of the chip. A real-time misalignment compensation procedure is used in the control software. The control software has its own script language, and it is also downward compatible with the script language used by the *Restructurable Wafer Editor* (RWED) used by MIT Lincoln Labs[2].

Ideally, chips that are fabricated in any foundry using standard processes that are used in the industry and have a particular interconnect structure (e.g., LDL) in them can be customized by having the laser simply create the interconnect (link or cut). If the electrical characteristics of the laser formed link emulate a standard foundry via without shifts in properties, all that is being done is emulating the section of the via mask for the interconnecting cell. Thus, interconnecting vias can be replaced by link structures.

E. User Friendly Operator Interface

The controlling software provides a very user-friendly operator interface through the use of mouse support, pull-down menus, and control panels. Pull-down menus organize the operational sequence while the control panels supply buttons, lists, custom displays, indicators, requestors, and comprehensive and user enhanced on-line help; all in a windows-like environment. The help facility is user enhanced, because the users can tailor the help files to meet their specific needs and taste. The help files are standard ASCII text files which can be edited with any DOS ASCII editor. In addition to editing files, control screens can be edited; providing an easy way to modify the functionality of the software without changing a single line of code. Gadgets (buttons, switches, lists, etc.) can be sized, moved, and have their color and associated fonts changed without affecting the operation of the control program. Options can be disabled directly on the control panel allowing any number of configurations. The ease of use of the control software allows minimally trained personnel to run the laser operation; the learning curve is smooth and meets the demands of a production environment. Flexibility

and useability are just as important as maintainability in today's ever changing manufacturing environment.

F. Standardization

Standardization is possible by using off-the-shelf control hardware and software. In this facility, besides the equipment needed to execute the laser operations, control hardware was used from National Instruments. Programmable analog/digital control and data acquisition boards were put in place in the controlling computer. This computer is based on an Intel 486DX processor running at 50 MHz clock speed with 8 MegaBytes of RAM, and it runs under the Microsoft DOS operating system. The controlling software was written using National Instruments' Lab Windows software development system using a subset of the C programming language. High flexibility was achieved by using this environment. It allows pre-compiled object modules to be loaded into the control program at run time. The control program can be run either in an executable form from the operating system prompt or from within the development environment. Debugging through the use of dynamically introduced breakpoints and checkpoints to view variables contents, results in minimized software development time. *Standard operating procedures* (SOPs) were produced and drafted in *Department of Defense* (DoD) format.

III. CONCLUSIONS

An infrastructure was developed and described. It allows this laboratory to be a rapid prototyping facility. The components of the system were given, and the operation details were discussed. One of the important features of the system is that it is (largely) personnel independent. By using only off-the-shelf vendor supplied components, feasible evolution can be realized.

Of utmost importance in today's high tech and constantly changing environment is the ability to adapt. Through the design process, every component was selected knowing that product upgrades (hardware, firmware, and software), new technology, and generally smarter components would precipitate change.

As this paper is being written, system enhancement is in progress. An interface to the CAD system is being developed. The VLSI design CAD tool currently used is Cadence Synergy from Cadence Design Systems Inc., San Jose, California[3]. The proposed goal is to be able to execute laser restructuring (linking and cutting) by pointing and clicking from within the CAD tools at the layout level. A similar interface link for other CAD systems is envisioned in the future.

ACKNOWLEDGEMENTS

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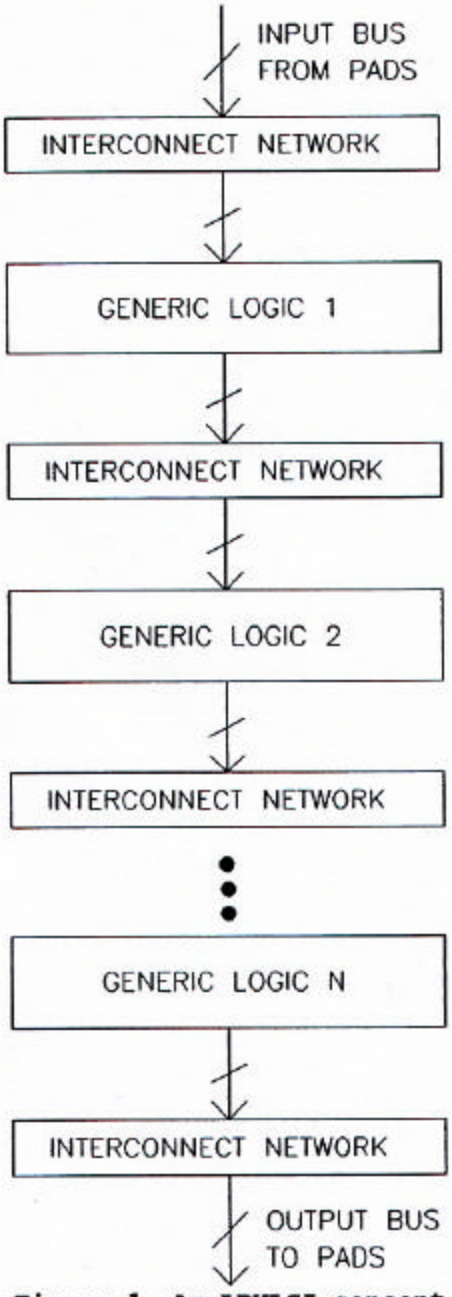

Figure 1 An LRVLSI concept

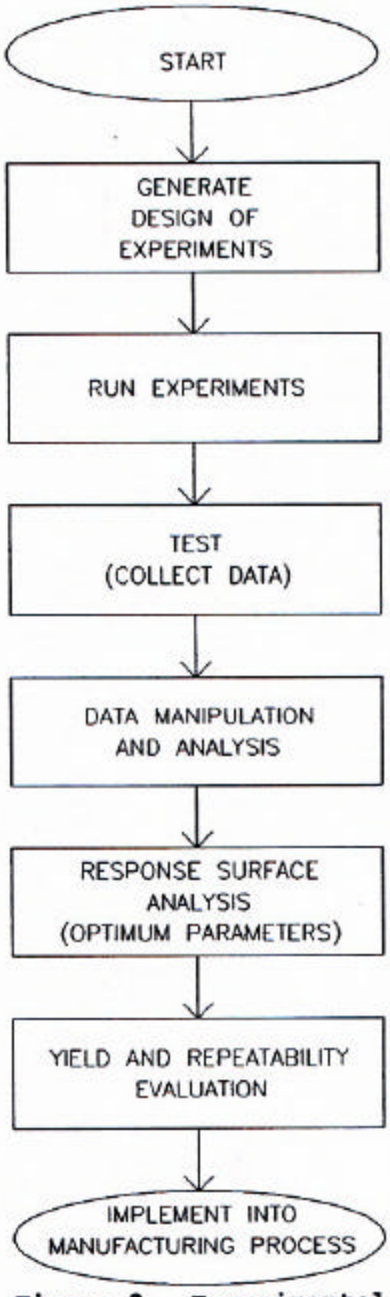

Figure 3 Experimental design flow

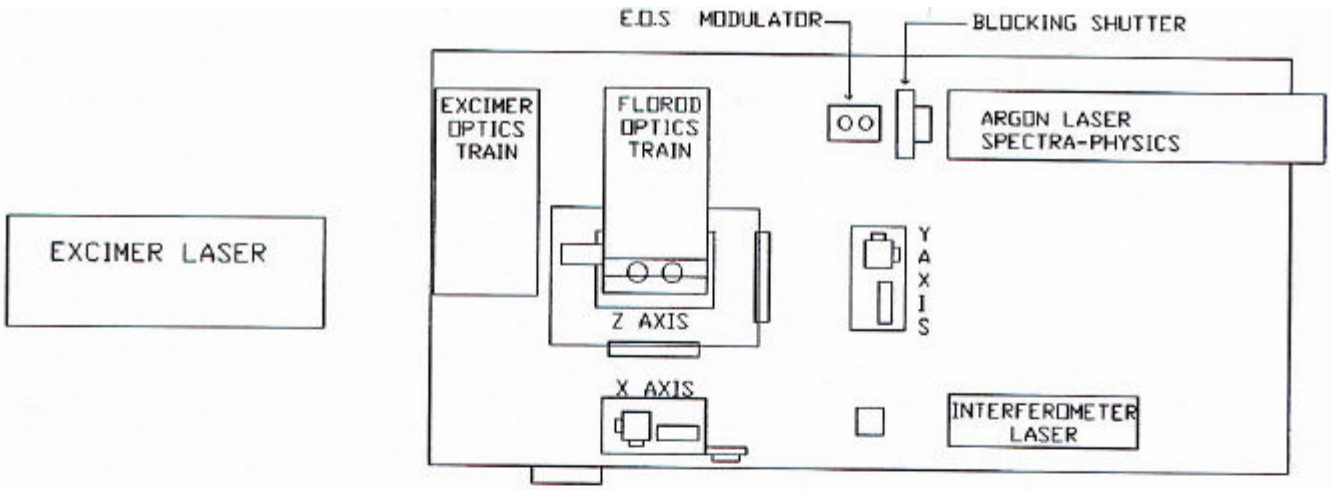

Figure 2 Laser restructuring table

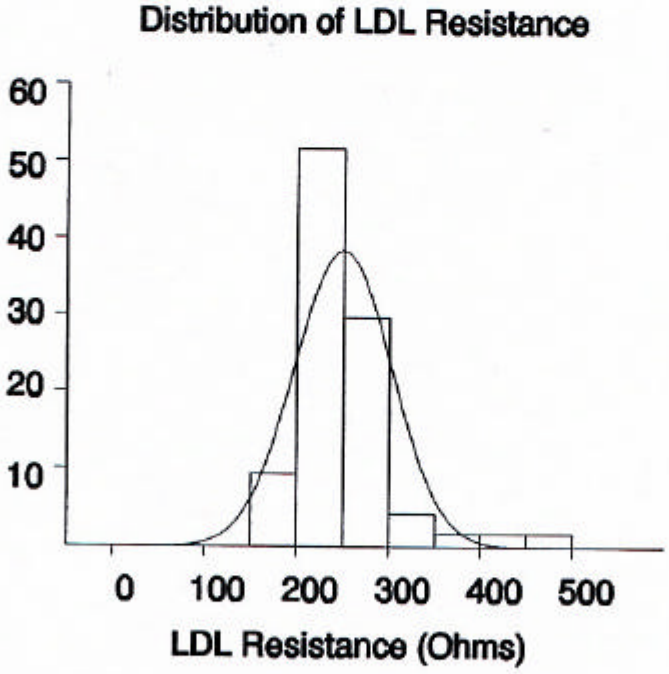

Figure 4 Distribution of LDL resistance