

**Orlando J. Hernandez, Ph.D.**

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**Highlights:**

- Teaching: VLSI Design, Digital Circuits and Microprocessors, Digital Image Processing, Computer Architecture and Organization.
- Experience with academic research in the areas of image processing and computer vision, and computer and VLSI architectures.
- Experience with guiding students in undergraduate student research projects in the areas of computer vision and related VLSI architectures with peer refereed published results.
- Experience with business management, program management, and chipset development - design and software integration at a system level.
- Experience with large team leadership and team work at a world wide level.
- Experience with embedded processors systems architecting.
- Experience with digital signal processing systems.
- Experience with development of highly integrated ASICs, high data bandwidth ASICs, and VLSI circuits for DSP.
- Experience with ASIC design using Verilog, VHDL, Synopsys family of tools, and back-end tools.
- Experience with C, C++, Unix software development utilities, and assembly language for generic processors and DSPs.
- Experience with MATLAB and Microsoft productivity tools.

**Academic Appointments:**

The College of New Jersey  
**Chair - Elec. & Computer Eng.** Ewing, New Jersey  
07/10 to present

The College of New Jersey  
**Associate Professor - Elec. & Computer Eng.** Ewing, New Jersey  
09/08 to present

The College of New Jersey  
**Assistant Professor - Elec. & Computer Eng.** Ewing, New Jersey  
08/03 to 08/08

Southern Methodist University  
**Guest Lecturer** Dallas, Texas  
08/01 to 08/03

Have been invited repeatedly as a guest lecturer for the Computer Vision course in the department of Electrical Engineering.

**Education:** Southern Methodist University Dallas, Texas  
**Doctor of Philosophy in Electrical Engineering** 05/2002  
Minor: Statistics.  
Area of Concentration: Image Processing and Computer Vision.  
Dissertation Title: Color Image Retrieval Using Multispectral Random Field Texture Models and Color Content Features.

University of South Florida Tampa, Florida  
**Master of Science in Electrical Engineering** 05/1993  
Area of Concentration: Digital and Analog VLSI Design for Communications and Digital Signal Processing.

University of South Florida Tampa, Florida  
**Bachelor of Science in Electrical Engineering** 12/1991  
GRADUATED MAGNA CUM LAUDE

**Awards:** EXTERNAL GRANTS (PI)  
GEARS SMP Surface Mobility Platform Robot  
\$ 1, 500 - Spring 2009  
GEARS-EDS Inc.

Precision Stabilization of a Ball Joint Gimbaled Mirror  
\$ 24, 870 - 8/1/07 to 3/1/08  
DSCI, US Navy STTR

Acquisition of Instrumentation Systems for Education and Research in Image Processing and Understanding  
\$ 93, 320 - 9/1/04 to 8/31/06  
National Science Foundation

CourseMaker Studio authoring suite. e-learning development and delivery tool  
\$ 3, 995 - Spring 2005  
Learn.com Inc.

TMS320C6701 Digital Signal Processor (DSP), and TMS320C6000 DSP Platform Code Composer Studio Development Tools and Software  
\$ 3, 679 - Spring 2005  
Texas Instruments Inc.

Xilinx DSP and Embedded Systems Design Tools and Software  
\$ 6, 864 - Spring 2005  
Xilinx Inc.

Xilinx Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) Development Tools and Software

\$ 3, 990 - Spring 2004

Xilinx Inc.

#### EXTERNAL FELLOWSHIPS

Selected as a participant in the 2004 Excellence in Engineering Education Teaching Workshop at the US Military Academy in West Point, NY. Selection was competitive for commitment to excellence in education. \$ 2, 500 - Summer 2004

#### TCNJ GRANTS

SOSA 2009-2010

SOSA 2008-2009

Student Summer Research 2008 - \$ 8,504

SOSA 2007-2008

Student Summer Research 2007 - \$ 6,000

SOSA 2006-2007

Student Summer Research 2006 - \$ 5,000

SOSA 2005-2006

Student Summer Research 2005 - \$ 10,000

MINI-GRANT - \$ 929 - Spring 2005

#### OTHER AWARDS

One of the recipients of the New Jersey Technology Award for Excellence in Technology from the New Jersey Technology Council. This award is based on the work of faculty members using technology in the classroom.

**Publications:** *Head Tracking System for Games and Simulations*  
The SPRING 9th International Conference on Computing, Communications and Control Technologies: CCCT 2011, March 27-30, 2011, Orlando, Florida

*High-Performance VLSI Architecture for the Microsoft® HD Photo Image Compression Algorithm*

The International Multi-Conference on Complexity, Informatics and Cybernetics, April 6-9, 2010, Orlando, Florida

*Precision Stabilization Simulation of a Ball Joint Gimbaled Mirror Using Advanced MATLAB(R) Techniques*

IEEE Southeast Conference 2009, March 5-8, 2009, Atlanta, Georgia

*An Autonomous Off-Road Robot Based on Integrative Technologies*

IEEE/ASME International Conference of Advanced Intelligent Mechatronics, July 2-5, 2008, Xi'an, China

*A Low Cost Advanced Encryption Standard (AES)*

*Co-Processor Implementation*

Journal of Computer Science and Technology, Volume 8, Number 1, April 2008

*An FPGA Architecture for Low Density Parity Check Codes*

IEEE Southeast Conference 2008, April 3-6, 2008, Huntsville, Alabama

*A Combined VLSI Architecture for Nonlinear Image Processing Filters*

IEEE Southeast Conference 2006, March 31 - April 2, 2006, Memphis, Tennessee

*A High Performance VLSI Architecture for the Histogram*

*Peak-Climbing Data Clustering Algorithm*

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 14, Number 2, February 2006

*A Classification Methodology for Color Textures Using Multispectral Random Field Mathematical Models*

Mathematical and Computational Applications, Volume 11, Number 2, 2006

*Face Recognition Using Multispectral Random Field Texture Models, Color Content, and Biometric Features*

34th Applied Imagery Pattern Recognition Workshop, October 19-21, 2005, Washington, DC

*Taking Advantage of Low Enrollment Scheduled Courses for the Integration of Research and Teaching*

35th ASEE/IEEE Frontiers in Education Conference, October 19-22, 2005, Indianapolis, Indiana

*Classification of Color Textures with Random Field Models and Neural Networks*

Journal of Computer Science & Technology, Volume 5, Number 3, October 2005

*C++ Encapsulated Dynamic Runtime Power Control for Embedded Systems*

IEEE Southeast Conference 2005, April 8-10, 2005, Fort Lauderdale, Florida

*Low-Cost Advanced Encryption Standard (AES) VLSI Architecture: A Minimalist Bit-Serial Approach*

IEEE Southeast Conference 2005, April 8-10, 2005, Fort Lauderdale, Florida

*High Performance VLSI Architecture for Data Clustering Targeted at Computer Vision*

IEEE Southeast Conference 2005, April 8-10, 2005, Fort Lauderdale, Florida

*Color Image Segmentation Using Multispectral Random Field Texture Model & Color Content Features*

Journal of Computer Science & Technology, Volume 4, Number 3, October 2004

*A Case Study on Teaching Design to Undergraduates: A Comprehensive First Course in VLSI Design*

International Conference on Engineering Education 2004, October 16-21, 2004, Gainesville, Florida

*An Image Retrieval System Using Multispectral Random Models, Color, and Geometric Features*

33rd Applied Imagery Pattern Recognition Workshop, October 13-15, 2004, Washington, D.C.

*Teaching Comprehensive Real World VLSI Design to Undergraduate Students*

2004 National Conference: Integrating Practice into Engineering Education, October 3-5, 2004

University of Michigan-Dearborn, Dearborn, Michigan

*Color Image Retrieval Using Multispectral Random Field Texture Model & Color Content Features*

Pattern Recognition Journal, Volume 36, Issue 8, August 2003  
Elsevier Science B.V. and the Pattern Recognition Society

*Color Image Retrieval Using Multispectral Random Field Texture Models and Color Content Features*

Dissertation, Spring 2002  
Southern Methodist University

*Color Image Retrieval Using Multispectral Random Field Texture Models*

IEEE Digital Signal Processing Workshop, October 15-18, 2000, Hunt, Texas

*Color Image Database Browsing and Retrieval using Multispectral Random Field Texture Models*

Research Day Conference, Spring 2000  
Southern Methodist University

*Integration of a Single-Chip Hard Disk Drive Controller Using Intellectual Property Modules*

14th TI-Japan Technical Conference, November 17, 1997  
Texas Instruments Inc.

*The UltraSPARC-I data buffer: TI ASIC's first 0.5 um-class product*

Texas Instruments Technical Journal, May-June 1996  
Texas Instruments Inc.

*Phase Locked Loop (PLL) Characterization Techniques*

Internal Paper, July 15, 1995  
Texas Instruments Inc.

*Contemporary ASIC Design Methodologies*

Internal Paper, November 11, 1994  
Texas Instruments Inc.

*A Parametric Logic Synthesis System for Nonlinear Mathematical Functions*

Internal Paper, March 21, 1994  
Texas Instruments Inc.

*Using MATLAB for Algorithm Development and Performance Analysis:  
A Coordinate Mapping for a Rapid Prototyping System*  
1993 MATLAB Conference, Proceedings, October 18-20, 1993,  
Cambridge, Massachusetts

*Rapid Prototyping Using Laser Restructuring VLSI Circuits*  
4th International Workshop on Rapid System Prototyping,  
Proceedings, June 28-30, 1993, Research Triangle Park, North  
Carolina

### Industry Experience:

Maxim Integrated Products, Inc. - uController Business Dallas, Texas  
**Technical Business Manager** 07/02 to 08/03

- Responsible for product definition to architect single chip microcontroller and DSP systems with analog content, as well as formulating business plans for each development program.
- Responsible for the following end equipments: electricity metering, safety system such as CO detectors and O2 monitors, hearing aids, networked media appliances, and digital audio players.

Texas Instruments, Inc. - Imaging & Audio Group Dallas, Texas  
**Design & Development Director** 04/00 to 07/02

- Managed a large team of engineers developing next generation Digital Imaging and Internet Audio DSP platforms. These designs contain DSP core and memory, microcontroller, co-processors, and peripherals. Data conversion, analog, and on-chip software are included in the system level integration as well (System-on-a-Chip).
- Drove full technology entitlement and very aggressive time to market and profitability cycle times.
- Drove chip set roadmap for the business unit.
- The group is divided in different functional sub-team: Systems/architecture/software, design, platform hardware, and product engineering.
- The group is divided in sub-teams across several regions of the world: US, Japan, and India.

Texas Instruments, Inc. - Imaging & Audio Group Dallas, Texas  
**Streaming Media Business Manager** 05/01 to 11/01

- Managed a group chartered with developing and marketing chipsets for Streaming Media end equipments. This team has the responsibility of defining a common platform for audio and imaging; then promote its wide adoption by 3rd parties, system houses, and customers. Ultimately, responsibility for development, execution, and marketing of the product fall within this group as well.

Texas Instruments, Inc. - ASIC/SLI Development      Dallas, Texas  
**Design Manager**      05/97 to 04/00

- Integrated a single chip system for a hard disk drive that contained a micro-controller, memories (including embedded flash), and ASIC logic.
- Interfaced with the customer to architect the integrated system solution.
- Led a team of design engineers engaged in the design of micro-controllers for hard disk drives, and the integration of hard disk drive ASICs.
- Led a team of design engineers developing micro-controllers for embedded system applications. The team is also responsible for the chip level design of some of the embedded systems. These were System-on-a-Chip class designs.

Texas Instruments, Inc. - Telecom Systems Division      Dallas, Texas  
**Digital Signal Processing Systems Engineer**      01/97 to 05/97

- Designed, coded, and tested Digital Signal Processing software for telecommunications systems platforms for voice recognition and speech processing with the TI TMS320C30 digital signal processor.

Texas Instruments, Inc. - ASIC Product Development      Dallas, Texas  
**Applications Engineer**      05/93 to 01/97

- Prototyped multiple hard disk drive controller ASICs.
- Performed the role of Program Manager, and led the development team working on the data buffer ASICs for the UltraSPARC (TM) processor.
- Developed and delivered training on ASIC products and libraries.
- Participated in the definition and development of ASIC products and libraries.

**Affiliations:** Membership in the ACM, the IEEE (Senior Member), along with the IEEE Computer Society and the IEEE Signal Processing Society, the American Society for Engineering Education, the National Society of Professional Engineers, and the Society of Hispanic Professional Engineers.

**Foreign Languages:**

Spanish	Can read, write, and speak fluently.
Japanese	Rudimentary.