FIGURE 5.44  A single-phase clock showing parameters of interest

Cycle Time ($T_C$)

Setup Time ($T_S$)

Hold Time ($T_H$)

Clock-to-Q Delay ($T_Q$)
FIGURE 5.49 Pipelined system options: (a) a register based pipelined system; (b) a latch based pipelined system; (c) another example of a latch based pipeline system.
FIGURE 5.57
Asynchronously settable
and resettable registers
FIGURE 5.60 Phase locked loops for clock synchronization: (a) a chip without a PLL and a potential skew problem; (b) a PLL-clock-generator solution to clock skew; (c) a clock-multiplying PLL; (d) another use of PLL clocks to synchronize data transfers between chips.
FIGURE 5.61 A charge pump PLL: (a) basic PLL block diagram; (b) typical CMOS VCO circuit; (c) typical CMOS VCDL circuit
FIGURE 5.63  A typical register based synchronizer
FIGURE 5.82 Clock-tree layout

delay have to match between stages
FIGURE 5.83  I/O pad options: (a) pad spacing; (b) interdigitated pads; (c) core limited pads; (d) pad limited pads; (e) solder bump I/O
FIGURE 5.86  Input pad electrostatic discharge (ESD) protection

typical input-protection circuits
FIGURE 5.89 A tristate pad (a) and a bidirectional pad (b)
**FIGURE 5.91** CMOS
Schmitt trigger circuit